

Application No.: 10/729,310

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**AMENDMENTS TO THE CLAIMS**

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (currently amended): A nonvolatile semiconductor memory device comprising:  
a memory cell array constituted by arranging a plurality of nonvolatile memory cells in a row direction and a column direction respectively and arranging the plurality of word lines and the plurality of bit lines in the row direction and the column direction respectively in order to select a predetermined memory cell or a memory cell group out of the arranged nonvolatile memory cells; wherein;

the memory cells are respectively constituted by connecting one end of a variable resistive element for storing information in accordance with a change of electrical resistances with the source of a selection transistor, [[and]]

in the memory cell array, the drain of the selection transistor is connected with a common bit line along the column direction, the other end of the variable resistive element is connected with a source line, and the gate of the selection transistor is connected with [[the]] a common word line along the row direction[.], and

the variable resistive element is a variable resistive element whose electrical resistance is changed due to an electrical stress.

Claim 2 (cancelled): The nonvolatile semiconductor memory device according to claim 1, wherein the variable resistive element is a variable resistive element whose electrical resistances are changed due to an electrical stress.

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Claim 3 (currently amended): The nonvolatile semiconductor memory device according to claim 1, wherein the variable resistive element is formed by a perovskite structural oxide containing manganese.

Claim 4 (currently amended): A nonvolatile semiconductor memory device comprising:  
a memory cell array constituted by arranging the plurality of nonvolatile memory cells in a row direction and a column direction respectively and arranging the plurality of word lines and the plurality of bit lines in the row direction and the column direction respectively in order to select a predetermined memory cell or a memory cell group out of the arranged nonvolatile memory cells;  
wherein

the memory cells are respectively constituted by connecting one end of a variable resistive element for storing information in accordance with a change of electrical resistances with the source of a first selection transistor and moreover connecting the other end of the variable resistive element with the drain of a second selection transistor, and

in the memory cell array, the drain of the first selection transistor is connected with a common bit line along the column direction, the source of the second selection transistor is connected with a source line, and gates of the first and second selection transistors are connected with a common word line along the row direction.

Claim 5 (original): The nonvolatile semiconductor memory device according to claim 4, wherein the variable resistive element is a variable resistive element whose electrical resistances are changed due to an electrical stress.

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Claim 6 (original): The nonvolatile semiconductor memory device according to claim 5, wherein the variable resistive element is formed by a perovskite-structural oxide containing manganese.

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